## **REMARKS**

The Examiner's Final Office Action mailed on December 3, 2003, has been received and its contents carefully considered.

Claims 21-27 and 42-52 are pending in this application. Claims 21 and 44 are amended herein.

In the Final Office Action, the Examiner for the first time rejects claims 21-27 and 42-52 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. In other words, the Examiner asserts that the claims contain subject matter, which was not described in specification in such a way as to reasonably convey to one, skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Specifically, regarding claims 21, 42-44 and 51-52, the Examiner notes that the claims recite: "...the back (or second) surface of the wafer exposed to convective air in the burn in apparatus..." The Examiner asserts that the specification does not provide a clear, concise and full description of the above claim limitation. While acknowledging that on page 23, lines 25-30, the application describes ventilating through holes in the holding plate to help circulate air to the exposed wafer, the Examiner argues that it does not described that the air is being exposed to the back surface of the wafer as claimed.

Further, regarding claims 24, 26, 47 and 49, the Examiner notes that the claims recite: "...disposed over the back (or second) surface of the wafer a holding plate having a through hole..." The Examiner asserts that the specification does not provide a clear, concise and full description of the above claim limitation, either. While acknowledging that on page 23, lines 25-30, the application describes ventilating through holes in the holding plate to help circulate air to the exposed wafer, the Examiner argues that it does not described that the holding plate as being disposed over the back surface of the wafer as claimed.

The Examiner's §112, first paragraph, rejection is respectfully traversed. As the Examiner notes, the text at page 23, lines 25-30, of the application, with reference to Figure 13, discloses that a plurality of through holes 309b are formed at the holding plate 309, making it possible to expose the wafer to be measured 401 to the air that circulates through convection when, for instance, burn-in is implemented on the wafer to be

measured 401. What the Examiner fails to note, as disclosed in Figures 17, and in detail in Figure 18, and discussed on page 24, lines 17-31, is that when the wafer to be measured 401 is mounted into the burn-in apparatus, it is mounted with the plurality of electrodes 411b, which the claims define as being on the <u>front</u> (or first) surface of the wafer, facing the film 305 and circuit board 303, and with the opposite surface, which the claims define as the <u>back</u> (or second) surface of the wafer, facing the holding plate 309, which has the plurality of through holes 309b.

Thus, when the application is considered as a whole, it is clear that the limitations "...with the back (or second) surface of the wafer exposed to convective air in the burn in apparatus..." and "...disposed over the back (or second) surface of the wafer a holding plate having a through hole..." are, in fact, disclosed in a manner so as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. Accordingly, the Examiner is respectfully requested to withdraw the §112, first paragraph, rejection, and to give appropriate patentable weight to these limitations in considering the pending claims.

In the present Action, the Examiner maintains the rejection of claims 21-27 and 42-52 under 35 USC 103(a) as being obvious over Nakata et al. (U.S. Patent No. 6,297,658) in view of Budnaitis et al. (U.S. Patent No. 5,896,038). The arguments advanced by the Examiner in support of rejection are very much the same as those contained in the previous Office Action dated May 7, 2003. The Applicant responded fully to those arguments in the Amendment filed on September 4, 2003, traversing the Examiner's obviousness rejection. For the sake of brevity, the remarks offered by the Applicant in the Amendment of September 4, 2003 are incorporated by reference as though fully set forth herein.

In Section 5 of the present Action, the Examiner indicates that the arguments offered by the Applicant in the Amendment of September 4, 2003 have been fully considered, but are not considered persuasive. Regarding claims 21 and 44, the Examiner acknowledges the Applicant's argument that Nakata fails to disclosed exposing the rear surface of the semiconductor wafer to air circulation, but, as noted above, declines to give patentable weight to the limitation "back surface" because there is allegedly no description given in the specification that the back of the wafer is being exposed to convective air, as claimed. The Applicant believes that the issue of support in the application for the "back

surface" limitation has been satisfactorily addressed and disposed of in the discussion above of the Examiner's §112, first paragraph, rejection.

The Examiner also dismisses the applicant's argument that Budnaitis fails to disclose cooling by exposing the back surface of the wafer to convective air in a burn-in apparatus, and that the forced air circulation suggesting in Budnaitis is significantly different from the convective cooling claimed in the present invention. While the Applicant does acknowledge that convection, which denotes the non-radiant exchange of heat between a surface and a fluid flowing over it, may involve either the free or forced movement of the fluid (see Parker, Concise Encyclopedia of Science and Technology, 3rd Ed., McGraw-Hill, 1994), neither of the references teaches exposing the back surface of the wafer to convective air in the burn-in apparatus. In Nakata, the burn in apparatus is sealed so that it can be evacuated (see, for example, column 6, lines 45-47), thus ruling out the use of holes in wafer tray 11 for convective cooling to the back of the semiconductor wafer 10 (see, for example, Figure 1). Budnaitis discloses that the wafer may be cooled by blowing cold air over the wafer (see column eight lines 46 49), but there is no suggestion of employing holes in the chuck 15 for convective cooling to the back of the semiconductor wafer 1 (see, for example, Figure 2). In this respect, Budnaitis is significantly different from the claimed invention.

Without prejudice to the applicant's traversal of the Examiner's §103(a) rejection, the Applicant amends claims 21 and 44 herein to further distinguish over the applied prior art references. As amended, claim 21 is directed to an invention in which the circuit elements are tested in a burn apparatus for electrical functions, positioning the semiconductor wafer in a positioning plate having a hole formed in a shape conforming to the shape of the semiconductor wafer, and exposing the back surface of the semiconductor wafer to convective air. As amended, claim 44 is directed to an invention in which circuit elements are tested in a burn in apparatus for electrical functions, positioning the semiconductor wafer in a positioning plate having a hole formed in a shape conforming to the shape of the semiconductor wafer, and exposing the second surface of the semiconductor wafer to convective air. The highlighted limitation is disclosed, for example, at page 23, lines 21-24, of the present application.

In the present invention, the terminals inputting/outputting functional test signals from a semiconductor device test apparatus can make contact with a plurality of electrodes formed on a semiconductor wafer surface (first surface) with a high degree of accuracy. The invention beneficially allows functional tests of each circuit element to be conducted effectively before dividing the semiconductor wafer into individual semiconductor devices, while controlling the temperature of the semiconductor wafer properly.

Nakata discloses, on the other hand, that the burn-in test is conducted in the wafer burn-in cassette by electrically connecting bumps 17 of the probe card 12 to the electrodes 16 formed in the surface of the semiconductor wafer 10 (see Figure 1, for example). However, Nakata discloses only that the burn in test is conducted when the semiconductor wafer 10 is mounted on the wafer tray 11 and fails entirely to disclose how the semiconductor wafer 10 is positioned on the wafer tray 11. As a result, in the burn-in test apparatus in Nakata, there is a significant possibility of misalignment and misconnection between the plurality of electrodes 16 formed on the semiconductor wafer 10 and the plurality of bumps 17 provided on the wiring board. Nakata lacks a positioning plate of the form recited, and is therefore quite different in structure from the presently claimed invention.

Budnaitis discloses, in column 8, lines 23-26, that "the wafer 1 may be held in the chuck 15 by a mechanical jig 16 and 17, by creating a vacuum (not shown) between the wafer 1 and the chuck 15," and in column 8, lines 46-48, that "the wafer may be cooled by blowing cold air over the wafer, by including a cooling element in the chuck 15."

However, Budnaitis only discloses that the wafer is held by the vacuum chuck or the mechanical chuck on the chuck 15, and entirely fails to disclose positioning the wafer in a positioning plate having a hole conforming in shape to the outer shape of the wafer, as claimed. As a result, in the burn in test apparatus of Budnaitis, there is a significant possibility of misalignment and misconnection between the plurality of contact pads 3 formed on the semiconductor wafer 1 and the plurality of bumps 18 provided on the contact sheet 9. Budnaitis, like Nakata, lacks a positioning plate of the form recited, and is therefore quite different in structure from the presently claimed invention.

In summary, Nakata and Budnaitis have structures that are quite different from each other, and neither discloses positioning a semiconductor wafer in a positioning plate

having a hole conforming to the outer shape of the semiconductor wafer. Accordingly, it is respectfully submitted that it would be impossible to achieve the structure of the present invention no matter how the references were to be combined.

For at least the foregoing reasons, it is respectfully submitted that independent claims 21 and 44, as well as their respective dependent claims, patentably distinguish over the applied art references, whether considered individually or a combination.

The Examiner's various rejections having been fully addressed, it is submitted that the application, as amended, is in condition for allowance. Entry of this Amendment and allowance of claims 21-27 and 42-52 is respectfully requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

Phillip G. Avrach-Reg. No. 46,076

RABIN & BÉRDO, P.C. CUSTOMER NO. 23995

Telephone: 202-371-8976

Telefax: 202-408-0924 E-mail: firm@rabinchamp.com

PGA:rw